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UTILITY PATENT APPLICATION TRANSMITTAL
(new nonprovisional applications under 37 CFR 1.53(b))

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First Named Inventor: Gregory Michael Wilson, et al.
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Title: A METHOD AND APPARATUS FOR FORMING A SILICON WAFER WITH A DENUDED ZONE

TO: ASSISTANT COMMISSIONER FOR PATENTS
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Washington, D.C. 20231

APPLICATION ELEMENTS

1. [ ] Fee Transmittal Form
(original and duplicate)

2. [X] Specification [Total Pages 25]

3. [X] Drawings [Total Sheets 4]

4. Oath or Declaration [Total Pages 4]

   a. [ ] Newly executed (original or copy)
   [X] New (unexecuted)

b. [ ] Copy from a prior application
(for continuation/divisional with Box 17 completed)

i. [ ] DELETION OF INVENTOR(s)
Signed statement attached deleting inventor(s) named in prior application.

5. [ ] Incorporation By Reference
(useable if Box 4b is marked)

The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program (Appendix)

7. [ ] Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)

a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))

9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney

10. [ ] English Translation Document (if applicable)

11. [ ] IDS with PTO-1449 [ ] Copies of IDS Citations

12. [ ] Preliminary Amendment

13. [X] Return Receipt Postcard

14. [ ] Small Entity Statement(s)

[ ] Statement filed in prior application; status still proper and desired

15. [ ] Certified Copy of Priority Document(s) if foreign priority is claimed

16. [ ] Other: _____

IF A CONTINUING APPLICATION, CHECK APPROPRIATE BOX AND SUPPLY THE REQUISITE INFORMATION BELOW AND IN A PRELIMINARY AMENDMENT

17. [ ] Continuation [ ] Divisional [ ] Continuation-in-Part

of Prior Application No.: ___/_____

Prior Application Examiner: _____

Group/Art Unit: _____

[ ] Complete Application

Based on provisional Application No. ___/_____

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A METHOD AND APPARATUS FOR FORMING A SILICON WAFER WITH A DENUDED ZONE

BACKGROUND OF THE INVENTION

The present invention generally relates to a method and apparatus for the preparation of semiconductor material substrates, especially silicon wafers, which are used in the manufacture of electronic components. More particularly, the present invention relates to a single crystal silicon wafer and a method for the preparation thereof. Such wafers include a denuded zone of an ideal, non-uniform depth distribution of oxygen precipitates formed during the heat treatment cycles of essentially any electronic device manufacturing process. Additionally, the wafer may comprise at least one major surface having an epitaxial silicon layer deposited thereon,

Single crystal silicon, which is the starting material for most processes used to fabricate semiconductor electronic components, is commonly prepared by using the Czochralski ("Cz") process. In this method, polycrystalline silicon ("polysilicon") is charged to a crucible and melted, a seed crystal is brought into contact with the molten silicon, and a single crystal is grown by slow extraction. The first portion of the crystal to be formed during the extraction process is a thin neck. After formation of the neck is complete, the diameter of the crystal is enlarged by decreasing the pulling rate and/or the melt temperature until the desired or target diameter is reached. A cylindrical main body of the crystal which has an approximately constant diameter is then grown by controlling the pull rate and the melt temperature while compensating for the decreasing melt level. Near the end of the growth process, but before the crucible is emptied of molten silicon, the crystal diameter is reduced gradually to form an end-cone. Typically, the end-cone is formed by increasing the crystal pull rate and heat supplied to the crucible. When the diameter becomes small enough, the crystal is then separated from the melt.

A number of defects in single crystal silicon form in the crystal growth chamber as the crystal cools after solidification. Such defects arise, in part, due to the presence of an excess (*i.e.*, a concentration above the solubility limit) of intrinsic point defects, which are known as crystal lattice vacancies and silicon self-interstitials. Silicon crystals grown from a melt are typically grown with an excess of one or the other type of intrinsic point

defect. It has been suggested that the type and initial concentration of these point defects in the silicon are determined at the time of solidification and, if these concentrations reach a level of critical supersaturation in the system and the mobility of the point defects is sufficiently high, a reaction (or an agglomeration event) will likely occur. The density of agglomerated intrinsic point defects in Cz silicon is conventionally within the range of about $1x10^3/cm^3$ to about $1x10^7/cm^3$. While these values are relatively low, agglomerated intrinsic point defects are of rapidly increasing importance to device manufacturers and, in fact, are now seen as yield-limiting factors in device fabrication processes and can severely impact the yield potential of the material in the production of complex and highly integrated circuits.

One particularly problematic type of defect is the presence of crystal originated pits ("COPs"). The source of this type of defect is the agglomeration of silicon lattice vacancies. More specifically, when silicon lattice vacancies agglomerate within a silicon ingot, they form voids. Subsequently, when the ingot is sliced into wafers, these voids are exposed and appear as pits on the wafer surfaces. These pits are referred to as COPs.

To date, there generally are three main approaches to dealing with the problem of agglomerated intrinsic point defects. The first approach includes methods which focus on crystal pulling techniques in order to reduce the number density of agglomerated intrinsic point defects in the ingot. This approach can be further subdivided into those methods having crystal pulling conditions which result in the formation of vacancy dominated material, and those methods having crystal pulling conditions which result in the formation of self-interstitial dominated material. For example, it has been suggested that the number density of agglomerated defects can be reduced by (i) controlling v/G_0 (where v is the growth velocity and G_0 is the average axial temperature gradient) to grow a crystal in which crystal lattice vacancies are the dominant intrinsic point defect, and (ii) influencing the nucleation rate of the agglomerated defects by altering (generally, by slowing down) the cooling rate of the silicon ingot from about 1100°C to about 1050°C during the crystal pulling process. While this approach reduces the number density of agglomerated defects, it does not prevent their formation. As the requirements imposed by device manufacturers become more and more stringent, the presence of these defects will continue to become more of a problem.

Others have suggested reducing the pull rate during the growth of the body of the crystal to a value less than about 0.4 mm/minute. This suggestion, however, is also not satisfactory because such a slow pull rate leads to reduced throughput for each crystal puller. More importantly, such pull rates lead to the formation of single crystal silicon having a high concentration of self-interstitials. This high concentration, in turn, leads to the formation of agglomerated self-interstitial defects and all the resulting problems associated with such defects.

A second approach to dealing with the problem of agglomerated intrinsic point defects includes methods which focus on the dissolution or annihilation of agglomerated intrinsic point defects subsequent to their formation. Generally, this is achieved by using high temperature heat treatments of the silicon in wafer form. For example, in European Patent Application No. 503,816 A1, Fusegawa et al. propose growing the silicon ingot at a growth rate in excess of 0.8 mm/minute, and heat treating the wafers which are sliced from the ingot at a temperature in the range of 1150°C to 1280°C to reduce the defect density in a thin region near the wafer surface. The specific treatment needed will vary depending upon the concentration and location of agglomerated intrinsic point defects in the wafer. Different wafers cut from a crystal which does not have a uniform axial concentration of such defects may require different post-growth processing conditions. Further, such wafer heat treatments are relatively costly, have the potential for introducing metallic impurities into the silicon wafers, and are not universally effective for all types of crystal-related defects.

A third approach to dealing with the problem of agglomerated intrinsic point defects is the epitaxial deposition of a thin crystalline layer of silicon onto the surface of a single crystal silicon wafer. This process provides a single crystal silicon wafer having a surface which is substantially free of agglomerated intrinsic point defects. Use of the traditional epitaxial deposition techniques, however, substantially increases the cost of the wafer.

In addition to containing the above-discussed agglomerated point defects, single crystal silicon prepared by the Cz method also typically contains various impurities, among which is mainly oxygen. This contamination, for example, occurs while the molten silicon is contained in the quartz crucible. At the temperature of the silicon molten

mass, oxygen comes into the crystal lattice until it reaches a concentration determined by the solubility of oxygen in silicon at the temperature of the molten mass and by the actual segregation coefficient of oxygen in solidified silicon. Such concentrations are greater than the solubility of oxygen in solid silicon at the temperatures typical for the processes for the fabrication of electronic devices. Thus, as the crystal grows from the molten mass and cools, the solubility of oxygen in it decreases rapidly. This ultimately results in wafers containing oxygen in supersaturated concentrations.

Thermal treatment cycles which are typically employed in the fabrication of electronic devices can cause the precipitation of oxygen in silicon wafers which are supersaturated in oxygen. Depending on their location in the wafer, the precipitates can be harmful or beneficial. Oxygen precipitates located in the active device region of the wafer can impair the operation of the device. Oxygen precipitates located in the bulk of the wafer, however, are capable of trapping undesired metal impurities that may come into contact with the wafer. The use of oxygen precipitates located in the bulk of the wafer to trap metals is commonly referred to as internal or intrinsic gettering ("IG").

Historically, electronic device fabrication processes have included a series of steps which were designed to produce silicon having a region near the surface of the wafer which is free of oxygen precipitates (commonly referred to as a "denuded zone" or a "precipitate free zone") with the balance of the wafer (*i.e.*, the wafer bulk) containing a sufficient number of oxygen precipitates for IG purposes. Denuded zones have been formed, for example, in a high-low-high thermal sequence such as (a) oxygen out-diffusion heat treatment at a high temperature (>1100°C) in an inert gas for a period of at least about 4 hours, (b) oxygen precipitate nuclei formation at a low temperature (600 to 750°C), and (c) growth of oxygen (SiO_2) precipitates at a high temperature (1000 to 1150°C). *See, e.g.*, F. Shimura, *Semiconductor Silicon Crystal Technology*, pp. 361-367 (Academic Press, Inc., San Diego CA, 1989) (and the references cited therein).

More recently, however, advanced electronic device manufacturing processes, such as DRAM manufacturing processes, have begun to minimize the use of high temperature process steps. Although some of these processes retain enough of the high temperature process steps to produce a denuded zone and sufficient density of bulk precipitates, the tolerances on the material are too tight to render it a commercially viable product. Other

current highly advanced electronic device manufacturing processes contain no out-diffusion steps at all. Because of the problems associated with oxygen precipitates in the active device region, therefore, these electronic device fabricators must use silicon wafers which are incapable of forming oxygen precipitates anywhere in the wafer under their process conditions. As a result, all IG potential is lost.

SUMMARY OF THE INVENTION

Among the objects of the present invention is the provision of a single crystal silicon wafer which (a) forms an ideal, non-uniform depth distribution of oxygen precipitates during a heat treatment cycle of essentially any electronic device manufacturing process and may also (b) have an epitaxial surface that is free of crystal originated pits; and the provision of an apparatus that can form the denuded zone and epitaxial surface in one apparatus eliminating the need for transfer between equipment.

Briefly, therefore, this invention is directed to a single crystal silicon wafer comprising: (a) two major, generally parallel surfaces (*i.e.*, the front and back surfaces); (b) a central plane between the front and back surfaces; (c) a circumferential edge joining the front and back surfaces; (d) a surface layer which comprises the region of the wafer between the front surface and a distance, D_1, of at least about 10 μm measured from the front surface and toward the central plane; and (e) a bulk layer which comprises a second region of the wafer between the central plane and the first region. This wafer is characterized in that the wafer has a non-uniform distribution of crystal lattice vacancies, wherein the concentration of vacancies in the bulk layer are greater than the concentration of vacancies in the surface layer, the vacancies have a concentration profile in which the peak density of the vacancies is at or near the central plane, and the concentration of vacancies generally decreases from the position of peak density in the direction of the front surface of the wafer. In addition, the front surface of the wafer may have an epitaxial layer deposited thereon. This epitaxial layer has a thickness of from about 0.1 to about 2.0 μm.

An aspect of the present invention involves a method of producing a denuded zone in a semiconductor wafer in a chamber having a source of heat, a susceptor, a wafer support and a Bernoulli wand head. The method includes heating a semiconductor wafer

with opposite major surfaces in the housing to an elevated temperature of at least about 1175°C with a heat source, said semiconductor being supported by a support in a housing during said heating. Ceasing the heating and moving said heated wafer to a position out of conductive heat relationship with the support with a Bernoulli wand head. Cooling the heated wafer in the housing while holding said wafer out of conductive heat transfer relationship with the support at a rate of at least 10°C/sec until the wafer reaches a temperature of less than about 850°C thereby forming a denuded zone in the wafer.

A further aspect of the present invention includes the provision of an apparatus for processing semiconductor wafers to form a denuded zone. The apparatus includes a housing defining a chamber and having a door selectively movable between an open position and a closed position. A heat source operably associated with the chamber and a support is in the chamber for selectively supporting a wafer in the chamber to be heated by the heat source. Inlet means communicates with the chamber for selectively permitting introduction of a fluid into the chamber. A Bernoulli wand mechanism with a wand head is movably mounted in the chamber and operable for moving the wafer to a position out of conductive heat transfer relationship with the support during cooling of the wafer to form a denuded zone. Control means is operably connected to the Bernoulli wand mechanism for controlling movement of the wand head between a wafer pick up position and wafer cooling position and being operable to maintain said wafer at the cooling position for a predetermined cooling period.

Other objects and features will be in part apparent and in part pointed out hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows the preferred structure of a single crystal silicon wafer that may be used as the starting material in accordance with the instant invention.

Figure 2 shows an oxygen precipitate profile of a wafer which may be prepared in accordance with the preferred embodiment of the instant invention.

Figure 3 shows an oxygen precipitate profile of a wafer which may be prepared in accordance with a preferred embodiment of the instant invention where the starting material is a vacancy-rich single crystal silicon wafer.

Figure 4 is a schematic diagram of a device used to support wafers during processing in a chamber with the wafer positioned for heating.

Figure 5 is a schematic plan view of a housing with portions broken away to show a chamber in which the wafers are processed, the Bernoulli wand being shown in a retracted position.

Figure 6 is a schematic sectional side elevation view of a Bernoulli wand.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In accordance with one embodiment of the present invention, a novel and useful single crystal silicon wafer comprising at least one surface having an epitaxial silicon layer deposited thereon and at least one denuded zone that are formed in one device has been developed. The device and process will be described for the production of a wafer with an eptaxial coating, however, the wafer can be produced without this coating, forming a wafer with at least one denuded zone. The epitaxial surface of the wafer is free of crystal originated pits, and the wafer contains a "template" that determines (or "prints") the manner in which oxygen will precipitate when the wafer is heated during the electronic device manufacturing process. Thus, during a heating step of essentially any electronic device manufacturing process, the wafer will form (a) a denuded zone of sufficient depth, and (b) a wafer bulk containing a sufficient density of oxygen precipitates for IG purposes. Also in accordance with this invention, a novel method has been developed for preparing such a single crystal silicon wafer. This method may be completed in a matter of minutes using equipment which is in common use in the semiconductor silicon manufacturing industry and thus eliminating the need for one expensive piece of manufacturing equipment, an RTA.

A. Starting Material

The starting material for the ideal precipitating wafer of the present invention is a single crystal silicon wafer which has been sliced from a single crystal ingot grown in accordance with any of the conventional variations of the Cz crystal growing method. This method, as well as standard silicon slicing, lapping, etching, and polishing techniques, are well known in the art and disclosed, for example, in F. Shimura,

Semiconductor Silicon Crystal Technology (Academic Press, 1989); and *Silicon Chemical Etching*, (J. Grabmaier, ed., Springer-Verlag, New York, 1982).

Referring to Figure 1, the wafer 1 preferably has a front surface 3, a back surface 5, and an imaginary central plane 7 between the front and back surfaces. The terms "front" and "back" in this context are used to distinguish the two major, generally planar surfaces of the wafer 1. The front surface 3 of the wafer 1 (as that phrase is used herein) is not necessarily the surface onto which an electronic device will subsequently be fabricated, nor is the back surface 5 of the wafer 1 (as that phrase is used herein) necessarily the major surface of the wafer 1 which is opposite the surface onto which the electronic device is fabricated. In addition, because silicon wafers typically have some total thickness variation (TTV), warp, and bow, the midpoint between every point on the front surface and every point on the back surface may not precisely fall within a plane. As a practical matter, however, the TTV, warp, and bow are typically so slight that to a close approximation the midpoints can be said to fall within an imaginary central plane which is approximately equidistant between the front and back surfaces.

The wafer may contain one or more dopants to give the wafer various desired properties. For example, the wafer may be a P-type wafer (*i.e.*, a wafer which has been doped with an element from Group 3 of the Periodic Table, most typically boron) or an N-type wafer (*i.e.*, a wafer which has been doped with an element from Group 5 of the Periodic Table, most typically arsenic). Preferably, the wafer is a P-type wafer having a resistivity in the range of between about 0.01 and about 50 Ω-cm. In a particularly preferred embodiment, the wafer is a P-type wafer having a resistivity in the range of between about 1 and about 20 Ω-cm. In another particularly preferred embodiment, the wafer is a P-type wafer having a resistivity in the range of between about 0.01 and about 1.0 Ω-cm.

Because the wafer is prepared using the Cz method, it typically may have an oxygen concentration anywhere from about $5x10^{17}$ to about $9x10^{17}$ atoms/cm^3 (ASTM standard F-121-83). The oxygen precipitation behavior of the wafer becomes essentially decoupled from the oxygen concentration in the ideal precipitating wafer; thus, the starting wafer may have an oxygen concentration falling anywhere within or even outside the range attainable by the Cz method. In addition, depending on the cooling rate of the single

crystal silicon ingot from the melting point of silicon (*i.e.*, about 1410°C) through the range of between about 750°C and about 350°C, oxygen precipitate nucleation centers may form. The presence or absence of these nucleation centers in the starting material typically is not critical to the present invention provided that these centers are capable of being dissolved by heat-treating the silicon at temperatures not in excess of about 1250°C.

This invention is particularly useful when used with vacancy-rich wafer starting materials. The phrase "vacancy-rich wafers" refers to wafers that contain a relatively large number of crystal lattice vacancy agglomerations. These agglomerations typically have an octahedral structure. In the bulk of the wafer, these agglomerations form voids; whereas at the surface of the wafer, they form COPs. The density of crystal lattice vacancy agglomerations within vacancy-rich wafers is typically from about $5x10^5$ to about $1x10^6/cm^3$, and the area density of COPs on the surface of such wafers is typically from about 0.5 to about 10 COPs/cm^2. Because such wafers may be sliced from silicon ingots formed by relatively low-cost processes (*e.g.*, the traditional open-architecture Cz processes), these wafers are a particularly preferred starting material.

B. Epitaxial Deposition

The single crystal silicon wafer prepared in accordance with this invention may additionally comprise a surface having an epitaxial silicon layer deposited thereon. The epitaxial layer may be deposited onto the entire wafer, or, alternatively, onto only a portion of the wafer. Referring to Figure 1, the epitaxial layer preferably is deposited onto the front surface 3 of the wafer. In a particularly preferred embodiment, it is deposited onto the entire front surface 3 of the wafer. Whether it is preferred to have an epitaxial layer deposited onto any other portion of the wafer will depend on the intended use of the wafer. For most applications, the existence or non-existence of an epitaxial layer on any other portion of the wafer is not critical.

As noted earlier, single crystal silicon wafers prepared by the Cz method often have COPs on their surfaces. A wafer used for integrated circuit fabrication, however, generally is required to have a surface which is free of COPs. A wafer having such a COP-free surface may be prepared by depositing an epitaxial silicon layer onto the surface of the wafer. Such an epitaxial layer fills in the COPs and ultimately produces a smooth

wafer surface. This has been the topic of recent scientific investigations. *See* Schmolke et al., *The Electrochem. Soc. Proc.*, vol. PV98-1, p. 855 (1998); Hirofumi et al., *Jpn. J. Appl. Phys.*, vol. 36, p. 2565 (1997). COPs on a wafer surface may be eliminated by using an epitaxial silicon layer thickness of at least about 0.1 μm. Preferably, the epitaxial layer has a thickness in the range of between about 0.1 μm and about 2 μm. More preferably, the epitaxial layer has a thickness in the range of between about 0.25 and about 1 μm, and most preferably in the range of between about 0.65 and about 1 μm.

It should be noted that the preferred thickness of the epitaxial layer may vary if the epitaxial layer is used to impart electrical properties to the wafer surface in addition to eliminating COPs. For example, precise control of a dopant concentration profile near the wafer surface may be achieved using an epitaxial layer. Where an epitaxial layer is used for a purpose in addition to eliminating COPs, such a purpose may require an epitaxial layer thickness which is greater than the preferred thickness used to eliminate the COPs. In such an instance, the minimum thickness to achieve the additional desired effect preferably is used. Depositing a thicker layer on the wafer is generally less commercially desirable because forming the thicker layer requires a greater deposition time and more frequent cleaning of the reaction vessel.

If a wafer has a native silicon oxide layer (*i.e.*, a silicon oxide layer which forms on a silicon surface when it is exposed to air at room temperature and generally has a thickness of from about 10 to about 15 Å) on its surface, the silicon oxide layer preferably is removed from the surface of the wafer before the epitaxial layer is deposited onto the surface. As used herein, the phrase "silicon oxide layer" refers to a layer of silicon atoms which are chemically bound to oxygen atoms. Typically, such an oxide layer contains about 2 oxygen atoms per silicon atom.

In a preferred embodiment of this invention, removal of the silicon oxide layer is accomplished by heating the surface of the wafer in an oxidant-free atmosphere until the silicon oxide layer is removed from the surface. More particularly, the surface of the wafer is preferably heated to a temperature of at least about 1100°C, and more preferably to a temperature of at least about 1150°C. This heating preferably is conducted while exposing the surface of the wafer to an atmosphere comprising H_2 or a noble gas (*e.g.*, He, Ne, or Ar). More preferably, the atmosphere comprises H_2. Most preferably, the

atmosphere consists essentially of H_2 because use of other atmospheres tends to cause etch pits to form in the surface of the wafer.

Traditionally, epitaxial deposition protocols, which remove a silicon oxide layer by heating a wafer in the presence of H_2, include heating the wafer to a high temperature (*e.g.*, from about 1000 to about 1250°C) and then baking the wafer at that temperature for a period of time (*e.g.*, typically up to about 90 seconds). It has been discovered, however, that if the surface of the wafer is heated to about 1100°C (and more preferably, about 1150°C), the silicon oxide layer is removed without the subsequent bake step, thereby eliminating the need for the bake step. Elimination of the bake step shortens the time required to prepare the wafer, and therefore is commercially desirable.

In a preferred embodiment of this invention, it is preferable to heat the wafer surface to remove the silicon oxide layer and then initiate silicon deposition less than 30 seconds (more preferably within about 10 seconds) after the silicon oxide is removed. Generally, this may be accomplished by heating the wafer surface to a temperature of at least about 1100°C (more preferably at least about 1150°C) and then initiating the silicon deposition less than 30 seconds (more preferably within about 10 seconds) after the wafer surface reaches that temperature. Waiting to initiate silicon deposition for up to about 10 seconds after removal of the silicon oxide layer allows the temperature of the wafer to stabilize and become uniform.

During the removal of the silicon oxide layer, the wafer preferably is heated at a rate which does not cause slip. More specifically, if the wafer is heated too quickly, a thermal gradient will develop which will create an internal stress sufficient to cause different planes within the wafer to shift relative to each other (*i.e.*, slip). Lightly doped wafers (*e.g.*, a wafer doped with boron and having a resistivity of about 1 to about 10 Ω-cm) have been found to be particularly susceptible to slip. To avoid this problem, the wafer preferably is heated in a heating apparatus or reactor, designated generally as 88, from room temperature to the silicon oxide removal temperature at an average rate in the range of between about 20 and about 35°C/sec. Preferably, this heating is accomplished by exposure to radiant heat such as light from halogen lights.

The epitaxial deposition preferably is carried out by chemical vapor deposition. Generally speaking, chemical vapor deposition involves exposing the surface of the wafer

to an atmosphere comprising silicon in an epitaxial deposition reactor or apparatus 88 which includes a housing 89, *e.g.*, an ASM Epsilon One, Model E2 EPI reactor (Advance Semiconductor Materials America, Inc., Phoenix, AZ). Such an apparatus 88 is described in copending patent application of Gregory W. Wilson, et al., serial no. 09/262,417, filed March 4, 1999, entitled Pressure Equalization System for Chemical Vapor Deposition Reactors, the disclosure of which is incorporated herein by reference. In a preferred embodiment of this invention, the surface of the wafer is exposed to an atmosphere comprising a volatile gas comprising silicon (*e.g.*, $SiCl_4$, $SiHCl_3$, SiH_2Cl_2, SiH_3Cl, or SiH_4). The gases or other fluids are introduced into the chamber through inlet means (not shown) communicating between a source of the fluid and the chamber. The process chamber 90 is defined by the housing 89 (Figure 5). The housing 89 includes a plurality of walls 91, 92, 93, 94, 95 and 96 defining the chamber 90. The housing 89 also includes at least one door 97 (both an inlet and outlet door 97 are shown) which is selectively open and closed and when closed the chamber 90 is sealed from the exterior so a pressure differential can be maintained with the exterior and/or prevent the ingress and egress of undesirable fluids during processing of the wafers. The illustrated housing 89 includes inlet and outlet load locks 98A, 98B respectively each with a door 97. The locks 98A, 98B are operable for holding wafers 1 for feeding to the process chamber 90 and for removal of finished wafers. The process chamber 90 may be divided into a treating station 90A, operable for heating and/or the deposition of the epitaxial coating, and a holding station 90B for both transferring and holding a wafer for cooling. It is to be understood that both epitaxial coating and wafer cooling can be done in a single chamber if desired. The housing 89 has mounted in the chamber 90 a Bernoulli wand mechanism 100 as is known in the art and is available with the above referenced ASM reactor. In the illustrated structure, the Bernoulli wand mechanism 100 has a head 130 that moves between the treating station 90A and holding station 90B. Movement of the Bernoulli wand 100 mechanism includes power operated means such as the extendable and retractable scissor arms 131 that are operably connected to and controlled by a control means 102 shown schematically in Figure 5, that is operable to effect and time the movement of the Bernoulli wand mechanism and the head 130 to remove a wafer from the inlet lock 98A, deposit the wafer 1 on a support 101 which includes a susceptor 103 which supports the

wafer 1 in a heating position, remove the wafer from the support and move the wafer to a cooling position, i.e., hold the wafer out of conductive heat transfer relation with the support for a predetermined period of time for cooling and deposit the finished wafer 1 in the outlet lock 98B. The control means 102 can include a programmable logic controller as are known in the art. The control means 102 can also be operably connected to the lamps 99 to control on and off timing and thereby heating of the wafer 1 by commencing heating for the epitaxial coating process and the increase of temperature and ceasing of heating to form the denuded zone(s). The atmosphere also preferably contains a carrier gas (preferably H_2). In one embodiment, the source of silicon during the epitaxial deposition is SiH_2Cl_2 or SiH_4. If SiH_2Cl_2 is used, the reactor vacuum pressure during deposition preferably is from about 500 to about 760 Torr. If, on the other hand, SiH_4 is used, the reactor pressure preferably is about 100 Torr. Most preferably, the source of silicon during the deposition is $SiHCl_3$. This tends to be much cheaper than other sources. In addition, an epitaxial deposition using $SiHCl_3$ may be conducted at atmospheric pressure. This is advantageous because no vacuum pump is required and the reactor chamber does not have to be as robust to prevent collapse. Moreover, fewer safety hazards are presented and the chance of air or other gases leaking into the reactor chamber is lessened.

During the epitaxial deposition, the temperature of the wafer surface preferably is maintained at a temperature sufficient to prevent the atmosphere comprising silicon from depositing polycrystalline silicon on the surface. Generally, the temperature of the surface during this period preferably is at least about 900°C. More preferably, the temperature of the surface is maintained in the range of between about 1050 and about 1150°C. Most preferably, the temperature of the surface is maintained at the silicon oxide removal temperature.

The rate of growth of the epitaxial deposition preferably is from about 3.5 to about 4.0 μm/min when the deposition is conducted under atmospheric pressure. This may be achieved, for example, by using an atmosphere consisting essentially of about 2.5 mole% $SiHCl_3$ and about 97.5 mole% H_2 at a temperature of about 1150°C and a pressure (absolute) of up to about 1 atm.

If the intended use of the wafer requires that the epitaxial layer include a dopant, the atmosphere comprising silicon also preferably contains the dopant. For example, it is often preferable for the epitaxial layer to contain boron. Such a layer may be prepared by, for example, including B_2H_6 in the atmosphere during the deposition. The mole fraction of B_2H_6 in the atmosphere needed to obtain the desired properties (*e.g.*, resistivity) will depend on several factors, such as the amount of boron out-diffusion from the particular substrate during the epitaxial deposition, the quantity of P-type dopants that are present in the reactor and substrate as contaminants, and the reactor pressure and temperature. An atmosphere containing about 0.03 ppm of B_2H_6 (*i.e.*, about 0.03 mole of B_2H_6 per 1,000,000 moles of total gas) at a temperature of about 1125°C and a pressure (absolute) of up to about 1 atm. to obtain an epitaxial layer having a resistivity of about 10 Ω-cm has been used.

Once an epitaxial layer having the desired thickness has been formed, the atmosphere comprising silicon preferably is purged with a noble gas (*e.g.*, Ar, Ne, or He) or H_2, and most preferably is purged with H_2. The wafer can then be heated, as described below to form the denuded zone(s) with no intervening cooling being needed.

C. Heat Treatment to Influence the Precipitation Behavior of Oxygen in the Wafer in a Subsequent Thermal Processing Step

In the embodiment of the invention utilizing epitaxial deposition, after epitaxial deposition, the wafer is treated to form a template of crystal lattice vacancies within the wafer which causes an ideal, non-uniform depth distribution of oxygen precipitates to form within the wafer when the wafer is heat-treated, such as during a heat treatment cycle of essentially any electronic device manufacturing process. In an alternate embodiment of the present invention, the formation of the epitaxial layer may be eliminated. Figure 2 shows one such oxygen precipitate distribution which may be formed using this invention. In this particular embodiment, the wafer 1 is characterized by regions 15 and 15' ("denuded zones") which are substantially free of oxygen precipitates. These zones extend from the front surface 3 and back surface 5 to a depth of t and t', respectively. Preferably, t and t' are each in the range of between about 10 and about 100 μm, and more preferably in the range of between about 50 and about 100 μm. Between the oxygen precipitate-free

regions 15 and 15', there is a region 17 which contains a substantially uniform concentration of oxygen precipitates. For most applications, the oxygen precipitate concentration in region 17 is at least about $5x10^8$ precipitates/cm^3, and more preferably is $1x10^9$ precipitates/cm^3. It should be recognized that the purpose of Figure 2 is to help acquaint those skilled in the art with this invention by illustrating merely one embodiment of this invention. This invention is not limited to that embodiment. For example, this invention may also be used to form a wafer having only one denuded zone 15 (instead of two denuded zones 15 and 15'). In a process where an epitaxial layer is formed, the temperature of the wafer with the epitaxial layer can be raised with no intermediate cooling step. In a process not utilizing an epitaxial deposition step, the wafer temperature is increased directly as described below.

To form the template of crystal lattice vacancies, the wafer generally is first heated in an oxidizing atmosphere comprising an oxidant, and then cooled at a rate of at least about 10°C/sec. The purpose of heating the wafer is to: (a) form self-interstitial and vacancy pairs (*i.e.*, Frenkel defects) in the crystal lattice which are distributed uniformly throughout the wafer, and (b) dissolve any unstabilized oxygen precipitate nucleation centers present in the wafer. Generally, heating to greater temperatures results in a greater number of Frenkel defects being formed. The purpose of the cooling step is to produce a non-uniform distribution of crystal lattice vacancies, wherein the vacancy concentration is maximum at or near the center of the wafer, and decreases in the direction of the surfaces of the wafer. This non-uniform distribution of crystal lattice vacancies is caused by the fact that a portion of vacancies near the surfaces of the wafer diffuse to the surfaces during the cool down and thereby become annihilated, resulting in lower concentrations of vacancies near the surfaces.

The non-uniform vacancy profile, in turn, is a template for oxygen precipitation when the wafer is subsequently heated as for example when making electronic components with the wafer. Specifically, when the wafer 1 (*see* Figure 2) is heated, oxygen will cluster rapidly to form precipitates 52 in the region 17 of the wafer 1 containing higher concentrations of vacancies, but will tend not to cluster in the regions 15 and 15' near the wafer surfaces 3 and 5 which contain lower concentrations of vacancies. Typically, the oxygen nucleates at temperatures in the range of between about 500°C and

about 800°C, and grows precipitates at temperatures in the range of between about 700°C and about 1000°C. Thus, for example, the non-uniform distribution of oxygen precipitates 52 in a wafer may be formed during a heat treatment cycle of an electronic device manufacturing process, given that such heat treatment cycles often are conducted at temperatures near 800°C.

As previously described, this invention may advantageously be used to treat a vacancy-rich wafer starting material, which has a relatively large number of COPs on its surface and voids within its bulk. Figure 3 shows the crystal lattice vacancy agglomerate 51 and oxygen precipitate 52 profile for an epitaxial wafer prepared from a vacancy-rich wafer starting material in accordance with this invention and then heat-treated to form oxygen precipitates. An epitaxial layer 50 is on the outer surfaces 3, 4, and 6 (no epitaxial layer is on the back surface 5 in this particular embodiment) of the wafer 1. Because the epitaxial layer has filled in the COPs, the wafer has smooth, COP-free surfaces 2 and 8. The profile of the oxygen precipitates 52 is similar to the oxygen precipitate profile in Figure 2, and is sufficient for intrinsic gettering. The profile of the vacancy agglomerates 51 completely within the bulk (*i.e.*, the profile of the voids within the bulk) of the wafer 1 essentially remains the same throughout the process of this invention (*i.e.*, the concentration remains about $5x10^4$ to about $1x10^6/cm^3$) and does not tend to affect the surfaces 2 and 8 of the wafer 1 due to the existence of the epitaxial layer 50 which acts as a barrier between the surfaces 2 and 8 and the agglomerates 51. Thus, the wafer making process is commercially useful, in part, because it enables the formation of a silicon wafer having intrinsic gettering ability and a COP-free surface from vacancy-rich starting material and one or more denuded zones, which wafer can be prepared with relatively low cost and with less capital equipment.

The heating and rapid cool-down to form the denuded zone(s) are preferably carried out in the epitaxial deposition reactor or housing 89. This eliminates the need for a second heating chamber and eliminates the handling of wafers to effect a transfer from an EPI chamber to an RTA. A heat source is operably associated with the housing 89 and the chamber 90 and as shown, includes one or more banks of high power lamps or lights 99, such as halogen lamps or lights mounted in the interior 90. Such lamps are used in rapid thermal annealing ("RTA") furnaces. The lamps 99 are capable of rapidly heating a

silicon wafer. For example, many are capable of heating a wafer from room temperature to 1200°C in a few seconds. Examples of commercially available RTA furnaces include model 610 furnace available from AG Associates (Mountain View, CA) and the CENTURA® RTP from Applied Materials (Santa Clara, CA). The lamps 99 are activated to heat the wafer 1 with energy from the light while the wafer is supported by the sususceptor 103 in the process position. The susceptor 103 and wafer 1 can be rotated while being heated by suitable drive means 104 connected to a shaft 105. Rotation helps achieve more uniform heating of the wafer 1 across its width. In one embodiment, the susceptor 103 is a graphite susceptor mounted on the shaft 105. The drive means 104 can include an electric motor. The lamps 99 may be the same ones that were used for the earlier heating steps to form the epitaxial layer. Referring to Figures 4 and 5, the apparatus 88 includes the susceptor 103 for supporting the wafer during heating to form the denuded zone 15, 15'. In order to effect the rapid cooling, the wafer 1 needs to be spaced from the susceptor 103 or other elements having high heat capacity at least during cooling. In the present invention, spacing for cooling is accomplished by the use of the Bernoulli wand 100 as described below. To improve the temperature uniformity across the width of the wafer, the susceptor 103 can be positioned adjacent to and in immediate radiant heat transfer relation with the wafer 1 during heating or processing. Immediate heat transfer relation shall include the wafer 1 being in contact with the susceptor 103 or spaced a distance therefrom of less than about 2 mm. The spacing between the wafer 1 and the susceptor 103 should be at least about 10mm during cooling where the wafer 1 and susceptor 103 are out of conductive heat transfer relation. It is desirable to use a susceptor 103 during heating of the wafer 1 to help distribute the heat more uniformly across the wafer.

As shown, the susceptor 103 is suitably supported in the chamber 90 by the shaft 105. The shaft 105 is shown as being connected to the motor 104 to be rotated thereby and thus rotate the susceptor 103 and wafer 1 thereon about a generally vertical axis. Alternatively, in some wafer processing, the wafer and hence the shaft and susceptor need not be rotated, eliminating the need for the motor 104. The susceptor 103 is mounted to shaft 105 via arms 107, which, in the illustrated structure, extend radially from the shaft 105 and are angularly spaced. Although any number of arms 107 can be provided, three

are used. The susceptor 103 is in spaced relation from the walls 91-96 and the door 97. The shaft 105 can be hollow to provide a pathway for thermocouple leads 110 for a thermocouple 112 mounted relative to the susceptor 103 to provide temperature information. The suspector 103 is located in an opening 112 in a floor 114 of the apparatus 88.

The cooling of the wafer needs to be rapid, at an average rate of at least about 10°C/sec, preferably at least about 15°C/sec, more preferably at least about 20°C/sec and still more preferably at least about 50°C/sec. The present invention achieves this by raising the wafer 1 off of the susceptor 103 and out of conductive heat transfer relation therewith. The Bernoulli wand 100 is well known in the industry and includes a hollow head 130 (Figure 6) connected in flow communication to a gas pump, shown schematically as 132, via the arms 131 that draw the gases from the chamber 90 and discharges them through a plurality of openings 133 in a lower surface 134 of the head 130 (see the flow arrows in Figure 6). When heating of the wafer 1 is completed, the Bernoulli wand head 130 moves into a position over the wafer 1, and lifts the wafer by directing gas flow across the wafer. The arms 131 are driven by a drive 135 under control of the controller 102. By being placed in proximity to a wafer 1, a pressure differential is created on opposite sides of the wafer 1 with the top surface 3 or 8 being exposed to a lower pressure than the back surface 5. The pressure differential effects movement of the wafer and when the pressure differential is correct, the wafer will float under the Bernoulli wand 100 exposing both sides of the wafer to the gaseous environment of the chamber 90. In this position, the wafer is out of conductive heat transfer relation with the susceptor 103 increasing the rate of heat loss for cooling. Further, the flow of gases from the Bernoulli wand provides forced convection heat transfer from the wafer 1 further increasing the rate of heat loss. Quick cooling is thus at least partially achieved by having a significant portion of the opposite faces 3, 5 or 8, 5 of the wafer 1 in contact with the gaseous environment of the chamber 90 and not a solid or high heat capacity support member. The cooling of the wafer 1 can occur in the chamber 90 and can occur in either the process station 90A or the holding station 90B. Heretofore, the Bernoulli wand was used to move the wafer before and after the epitaxial layer was formed. Also, formation of a denuded

zone and the epitaxial coating were done in separate chambers, not one chamber or apparatus as in a particularly preferred form of the present invention.

For most applications, the wafer 1 preferably is heated in the pre-existing atmosphere in the chamber 90 to form the denuded zone(s) to a soak temperature of at least about 1175°C. More preferably, it is heated to a soak temperature in the range of between about 1200°C and about 1250°C. Heating of the wafer 1 to form the denuded zone(s) is preferably achieved by increasing the temperature of the wafer 1 after the heating to form the epitaxial layer without an intervening cooling step. Once the temperature of the wafer 1 reaches the preferred soak temperature, the wafer temperature is preferably held at the soak temperature for a period of time. The wafer temperatures as disclosed herein are measured as a surface temperature with a temperature measuring device such as a pyrometer. The preferred amount of time generally is in the range of between about 10 and about 15 seconds. The wafer preferably is held at the soak temperature in the range of between about 12 and about 15 seconds. For slower cooling rates, the wafer may be heated at a higher temperature to generate a higher concentration of silicon lattice vacancies before the cool-down step.

Following the heat treatment of the wafer 1, the wafer is rapidly cooled as described above. This cooling step may conveniently be carried out in the housing 89 in which the heat-treatment is conducted. Alternatively, it preferably is carried out in an atmosphere which will not react with the wafer surface. The rapid cooling rate preferably is used as the temperature of the wafer decreases through the range of temperatures at which crystal lattice vacancies diffuse through the single crystal silicon. Once the wafer is cooled to a temperature outside the range of temperatures at which crystal lattice vacancies are relatively mobile, the cooling rate does not significantly influence the precipitating characteristics of the wafer, and, thus, is not narrowly critical. Generally, crystal lattice vacancies are relatively mobile at temperatures greater than about 850°C. It is preferred to fast cool the wafer to a temperature of less than about 850°C and preferably less than about 800°C

In a preferred embodiment, the average cooling rate of the wafer is at least about 10°C/sec. as its temperature falls from the soak temperature to a temperature which is at least about 325°C less than the denuded zone formation soak temperature. More

preferably, the average cooling rate of the wafer is at least about 15°C/sec. as its temperature falls from the soak temperature to a temperature which is at least about 325°C less than the soak temperature. Still more preferably, the average cooling rate of the wafer is at least about 20°C/sec. as its temperature falls from the soak temperature to a temperature which is at least about 325°C less than the soak temperature. Most preferably, the average cooling rate of the wafer is at least about 50°C/sec. as its temperature falls from the soak temperature to a temperature which is at least about 325°C less than the soak temperature.

In a particularly preferred embodiment, the average cooling rate of the wafer is at least about 10°C/sec. as its temperature falls from the denuded zone formation soak temperature to a temperature which is at least about 400°C less than the soak temperature. More preferably, the average cooling rate of the wafer is at least about 15°C/sec. as its temperature falls from the soak temperature to a temperature which is at least about 400°C less than the soak temperature. Still more preferably, the average cooling rate of the wafer is at least about 20°C/sec. as its temperature falls from the soak temperature to a temperature which is at least about 400°C less than the soak temperature. Most preferably, the average cooling rate of the wafer is at least about 50°C/sec. as its temperature falls from the soak temperature to a temperature which is at least about 400°C less than the soak temperature.

In another particularly preferred embodiment, the average cooling rate of the wafer is at least about 10°C/sec. as its temperature falls from the denuded zone formation soak temperature to a temperature which is at least about 450°C less than the soak temperature. More preferably, the average cooling rate of the wafer is at least about 15°C/sec. as its temperature falls from the soak temperature to a temperature which is at least about 450°C less than the soak temperature. Still more preferably, the average cooling rate of the wafer is at least about 20°C/sec. as its temperature falls from the soak temperature to a temperature which is at least about 450°C less than the soak temperature. Most preferably, the average cooling rate of the wafer is at least about 50°C/sec. as its temperature falls from the soak temperature to a temperature which is at least about 450°C less than the soak temperature.

When introducing elements of the present invention or the preferred embodiment(s) thereof, the articles "a", "an", "the" and "said" are intended to mean that there are one or more of the elements. The terms "comprising", "including" and "having" are intended to be inclusive and mean that there may be additional elements other than the listed elements.

As various changes could be made in the above constructions without departing from the scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

WHAT IS CLAIMED IS:

1. A method of producing a denuded zone in a semiconductor wafer in a housing having a source of heat, a susceptor, a wafer support and a Bernoulli wand, said method including:

heating a semiconductor wafer with opposite major surfaces in a housing to an elevated temperature of at least about 1175°C with a heat source, said semiconductor being supported by a support in the housing during said heating;

ceasing said heating and moving said semiconductor out of conductive heat transfer relation with the support with the Bernoulli wand; and

cooling said heated wafer in the housing while holding said wafer out of conductive heat transfer relationship with the support at a rate of at least 10°C/sec until the wafer reaches a temperature of less than about 850°C thereby forming a denuded zone in the wafer.

2. A method as set forth in claim 1 including placing the wafer in a chamber and applying an epitaxial coating to at least one said major surface thereof with said wafer being in immediate heat transfer relation with the support during at least a portion of the coating application;

3.A method as set forth in claim 3 wherein said wafer is heated to a temperature of at least about 1250°C after said coating is applied and the cooling rate of the wafer is at least about 20°C/sec.

4. A method as set forth in claim 2 wherein said wafer is cooled at a rate of at least about 15°C/sec.

5. A method as set forth in claim 2 wherein said wafer is cooled at a rate of at least about 20°C/sec.

6. A method as set forth in claim 2 wherein said wafer is cooled at a rate of at least about 50°C/sec.

7.A method as set forth in claim 4 wherein said cooling rate is at least about 15°C/sec until the temperature of the wafer is reduced at least about 325°C.

8. A method as set forth in claim 5 wherein said cooling rate is at least about 20°C/sec until the temperature of the wafer is reduced at least about 325°C.

9. A method as set forth in claim 6 wherein said cooling rate is at least about 50°C/sec until the temperature of the wafer is reduced at least about 325°C.

10. A method as set forth in claim 4 wherein said cooling rate is at least about 15°C/sec until the temperature of the wafer is reduced at least about 400°C.

11. A method as set forth in claim 5 wherein said cooling rate is at least about 20°C/sec until the temperature of the wafer is reduced at least about 400°C.

12. A method as set forth in claim 6 wherein said cooling rate is at least about 50°C/sec until the temperature of the wafer is reduced at least about 400°C.

13. A method as set forth in claim 4 wherein said cooling rate is at least about 15°C/sec until the temperature of the wafer is reduced at least about 450°C.

14. A method as set forth in claim 5 wherein said cooling rate is at least about 20°C/sec until the temperature of the wafer is reduced at least about 450°C.

15. A method as set forth in claim 6 wherein said cooling rate is at least about 50°C/sec until the temperature of the wafer is reduced at least about 450°C.

16. A method as set forth in claim 1 wherein said heat source is light.

17. A method as set forth in claim 16 wherein said heat source is a halogen lamp.

18. An apparatus for processing semiconductor wafers to form a denuded zone in the wafer, said apparatus comprising:

a housing defining a chamber and having a door selectively movable between an open position and a closed position;

a heat source operably associated with the chamber;

a support in the chamber for selectively supporting a wafer in the chamber;

inlet means communicating with the chamber for selectively permitting introduction of a fluid into the chamber;

a Bernoulli wand mechanism with a wand head movably mounted in the chamber and operable for moving the wafer to a position out of conductive heat transfer relationship with the support during cooling of the wafer to form a denuded zone; and

control means operably connected to the Bernoulli wand mechanism for controlling movement of the wand head between a wafer pick up position and wafer cooling position and being operable to maintain said wafer at the cooling position for a predetermined cooling period.

19. An apparatus as set forth in claim 18 wherein the door is operable for selectively sealing said chamber interior from an exterior of the chamber to maintain a pressure differential between the exterior and the chamber interior.

20. An apparatus as set forth in claim 19 wherein the support includes a susceptor positioned to be in immediate heat transfer relation with a wafer during heating of a wafer.

A METHOD AND APPARATUS FOR FORMING A SILICON WAFER WITH A DENUDED ZONE

Abstract of the Invention

An apparatus and method are provided for forming an epitaxial layer on and denuded zone in a semiconductor wafer used in manufacturing electronic components. The denuded zone and epitaxial layer are formed in one apparatus. The apparatus includes a Bernoulli wand that is used to support the wafer in a cooling position to effect fast cooling of the wafer and formation of the denuded zone.

FIG. 1

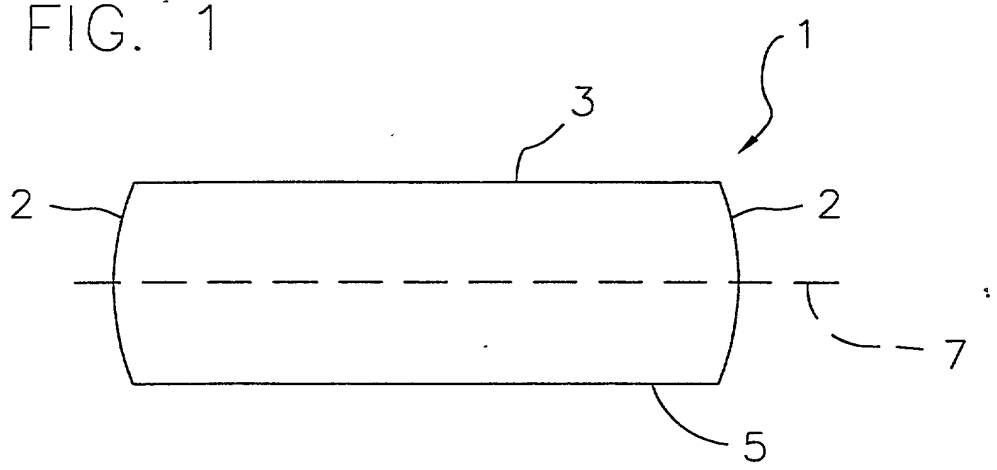


FIG. 2

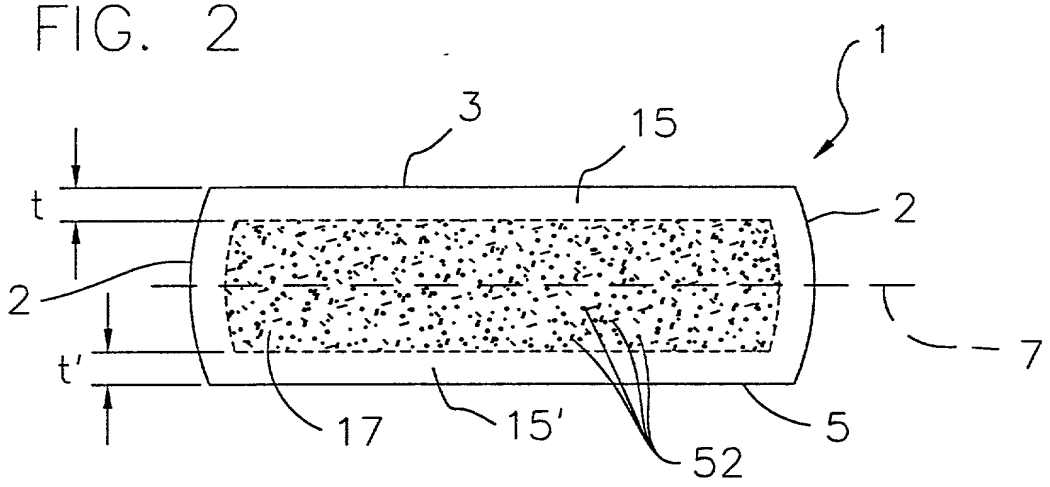
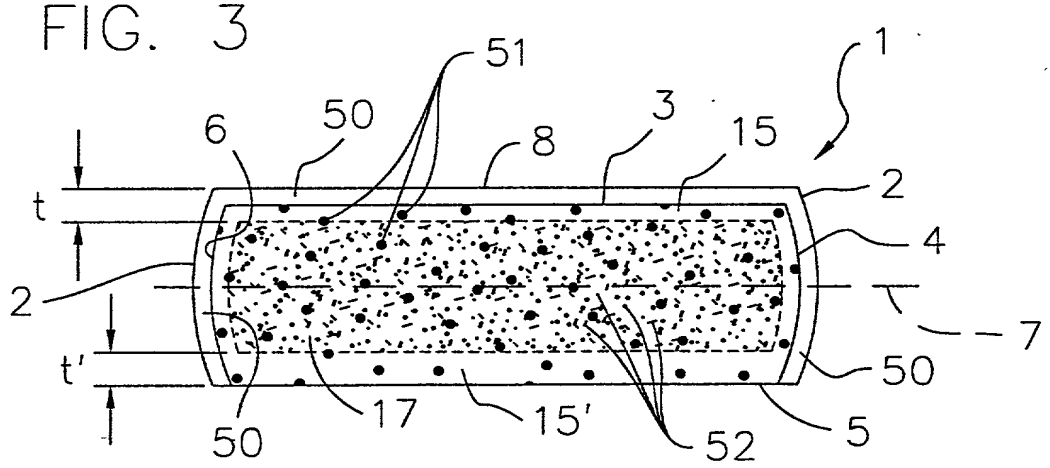


FIG. 3



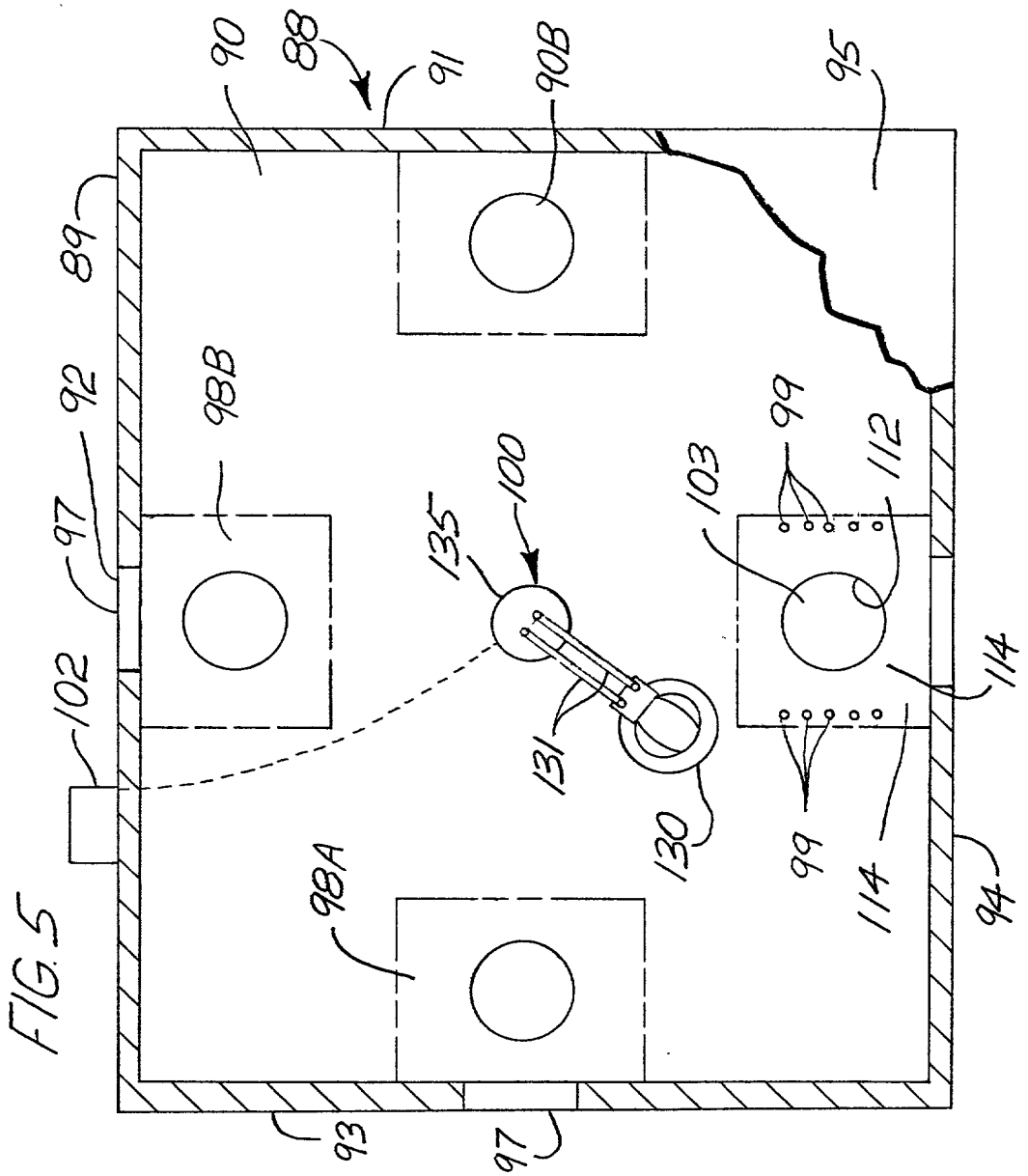

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FIG. 5

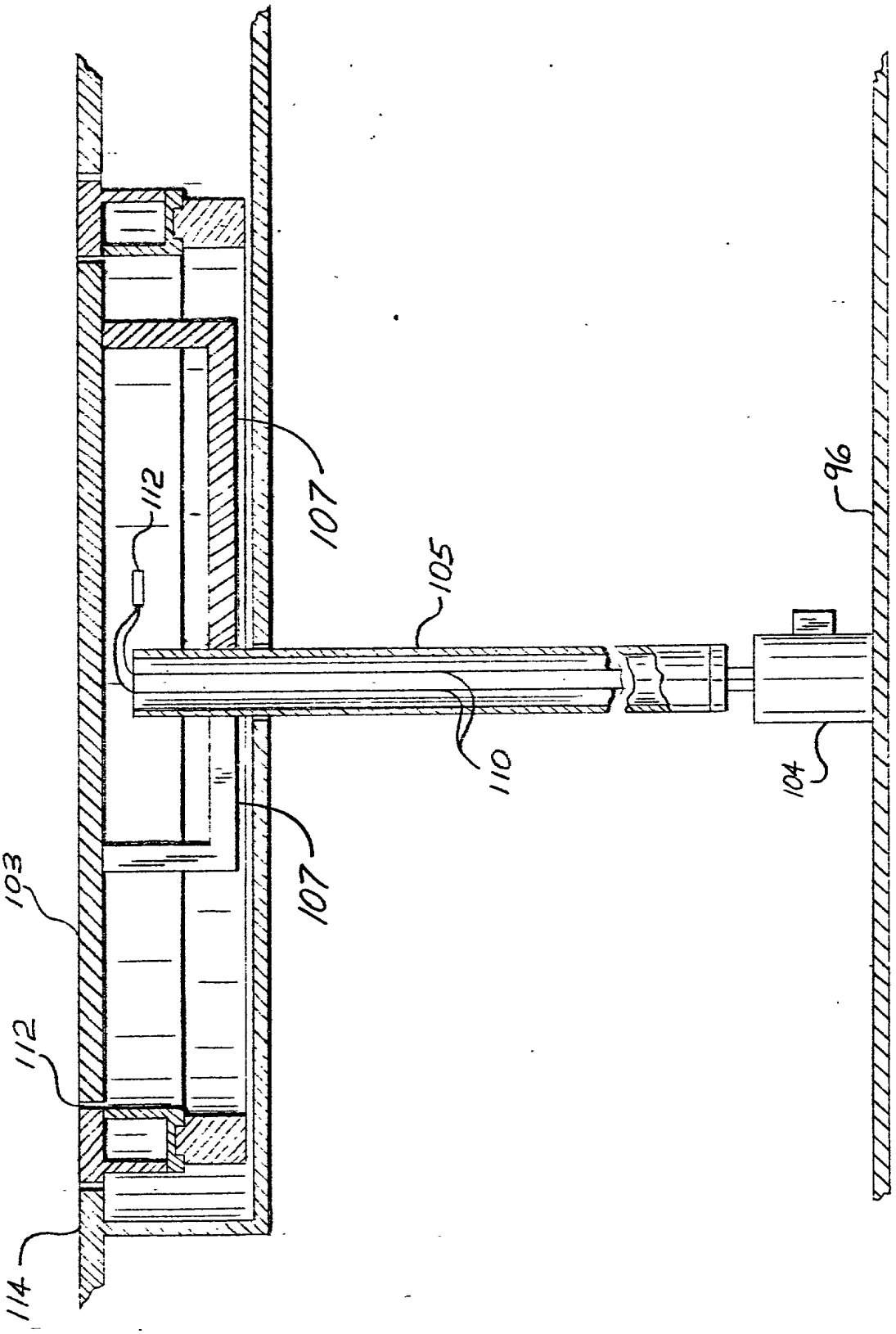

FIG. 4

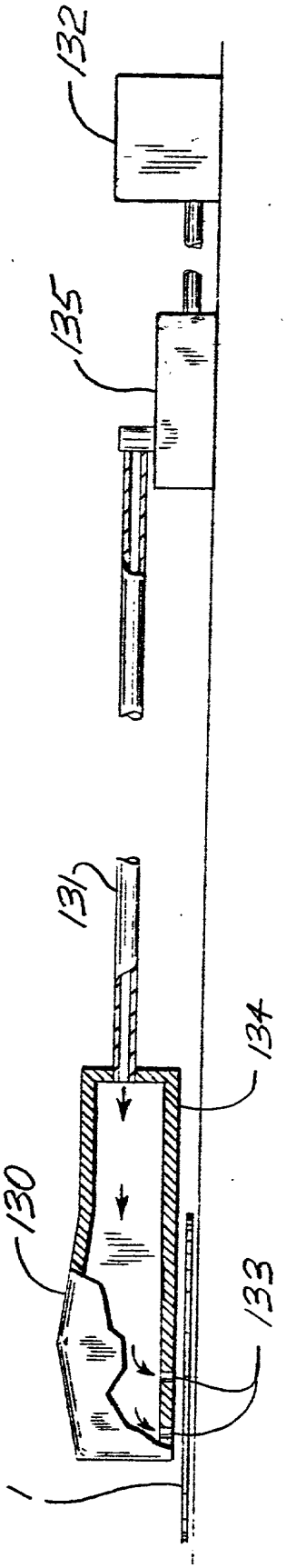

FIG. 6

Attorney's Docket No.: **TP-98-4650(MEMC 2293)**

DECLARATION AND POWER OF ATTORNEY

REGULAR OR DESIGN APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

A METHOD AND APPARATUS FOR FORMING A SILICON WAFER WITH A DENUDED ZONE

the specification of which:

(check one)

[X] is attached hereto

[ ] was filed on _____ as Application Serial No. _____, and was amended on _____.

[ ] was described and claimed in PCT International Application No. _____, filed on _____ and as amended under PCT Article 19 on _____, if any.

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a) - (d) or §365(b) of any foreign application for patent or inventor's certificate, or §365(a) of any PCT application which designates at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIORITY CLAIMED

(Number)	(Country)	(Day/Month/Year Filed)
(Number)	(Country)	(Day/Month/Year Filed)
(Number)	(Country)	(Day/Month/Year Filed)

PRIORITY NOT CLAIMED

ANY FOREIGN APPLICATION(S), ON THE SAME SUBJECT MATTER WHICH HAS A FILING DATE EARLIER THAN THE EARLIEST APPLICATION FROM WHICH PRIORITY IS CLAIMED

(Number)	(Country)	(Day/Month/Year Filed)

CLAIM FOR BENEFIT OF PROVISIONAL APPLICATION(S)

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

CLAIM FOR BENEFIT OF EARLIER U.S. APPLICATION(S) UNDER 35 U.S.C. 120

(complete this part only if this is a divisional, continuation or CIP application)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s), or §365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

POWER OF ATTORNEY

I hereby appoint the following attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Irving Powers (15,700), Donald G. Leavitt (17,626), John K. Roedel, Jr. (25,914), Michael E. Godar (28,416), Edward J. Hejlek (31,525), William E. Lahey (26,757), Richard G. Heywood (18,224), Frank R. Agovino (27,416), Kurt F. James (33,716), G. Harley Blosser (33,650), Paul I. J. Fleischut (35,513), Vincent M. Keil (36,838), Robert M. Evans, Jr. (36,794), Robert M. Bain (36,736), Joseph A. Schaper (30,493), Kathleen M. Petrillo (35,076), David E. Crawford, Jr. (38,118), Paul A. Maddock (37,877), Scott A. Williams (39,876), Richard L. Bridge (40,529), David M. Gryte (41,809), Christopher M. Goff (41,785), James E. Butler (40,931), Derick E. Allen (43,468), Matthew L. Cutler (43,574), Michael G. Munsell (43,820), Robert J. Lewis (27,210), Karen Y. Hui (44,785), Anthony R. Kinney (44,834), Brian P. Klein (44,837), Sarah J. Chickos (46,157), Donald W. Tuegel (45,424), Steven M. Ritchey (46,321), Michael J. Thomas (39,857), and Kathryn J. Doty (40,593), all of the law firm of SENNIGER, POWERS, LEAVITT & ROEDEL, One Metropolitan Square, 16th Floor, St. Louis, Missouri 63102.

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Customer Number: 000321	Kurt F. James (314) 231-5400

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

- -

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